Yufan Du

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Education

Peking UniversitySep. 2021 - PresentBachelor of Science in Applied Physics and Computer Science Dual MajorBeijing, China

Relevant Scores

Overall GPA:	3.850/4.000 (Rank: 3rd out of 64 students)
TOEFL:	108 (R27 + L30 + S23 + W28)
GRE:	324 (Quantitative170 + Verbal154), 4.0 (Analytical Writing)

Technical Skills

Knowledgeable with: C/C++, Python Familiar with: Python ML libraries (PyTorch, NumPy), Verilog, FPGA, Embedded systems, Linux systems, MATLAB, Tcl, LATEX, SQL/Database, JavaScript/HTML EDA tools: Familiar with Cadence Innovus, Cadence Virtuoso

Publications

- Yufan Du, Zizheng Guo, Yibo Lin, Runsheng Wang and Ru Huang, "Fusion of Global Placement and Gate Sizing with Differentiable Optimization," 2024 International Conference on Computer-Aided Design (ICCAD24). (best paper candidate of track).
- Zizheng Guo, Zuodong Zhang, Wuxi Li, Tsung-Wei Huang, Xizhe Shi, **Yufan Du**, Yibo Lin, Runsheng Wang and Ru Huang, "HeteroExcept: A CPU-GPU Heterogeneous Algorithm to Accelerate Exception-aware Static Timing Analysis," 2024 International Conference on Computer-Aided Design (ICCAD24).
- Yufan Du[†], Zizheng Guo[†], Xun Jiang, Zhuomin Chai, Yuxiang Zhao, Yibo Lin, Runsheng Wang and Ru Huang, "PowPrediCT: Cross-Stage Power Prediction with Circuit-Transformation-Aware Learning," 2024 Design Automation Conference (DAC24).

Project Experiences

FPGA-Based Gesture-Controlled Snake GameMar. 2023 - July. 2023

- Advisor: Professor Xiaohui Duan.

- Deployed *computer vision algorithms* (from Canny edge detection, circular hough transformation, to pattern recognization) and the classic Snake game on a resource-limited FPGA platform.

- Developed and implemented a *real-time control mechanism* with a camera detecting gestures.

- Provided insights for *IoT edge device*.

AI-Assisted Schedule Manager

- Advisor: Professor Wei Guo.

- Developed a *cross-platform application* integrated with commercial AI API for users' agenda scheduling.

- Better user experience through conversational interfaces for management and reminders.

Jan. 2023 - Apr. 2023

Research Experiences

Jun. 2024 - Sept. 2024

CUDA-Accelerated Gate Sizing - Advisor: Professor David Z. Pan.

- Served as the first author.

- For ICCAD 2024 contest problem C.

- CUDA programming to accelerate the gate sizing process with gradient descent method.

The Integration of Gate Sizing and Global Placement Dec. 2023 - May. 2024

- Advisor: Professor Yibo Lin.

- Served as the first author.

- A novel fusion of global placement and gate sizing with differentiable optimization for broader optimization space.

- Demonstrated a substantial improvement in runtime efficiency and PPA metrics compared to traditional methods.

- Accepted by ICCAD 2024 (Best paper candidate of track).

Cross-Stage Power Prediction for Integrated Circuits Jun. 2023. - Nov. 2023. - Advisor: Professor Yibo Lin.

- Served as the first author.

- ML prediction framework that integrates cross-stage circuit-transformation-aware learning.

- Achieved a significant reduction in error rates and computation time compared to industry-leading commercial tools.

- Accepted by DAC 2024.